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Nanoscale NMOS Device design and its electrical characteristics using Visual TCAD Tool in 3-D

[1]Palvinder Singh, [2]Sushil Kakkar and [3]Ravi Kant

[1,2,3]ECE Department, BGIET Sangrur

[1]*palvinder4us2006@gmail.com,*[2]*sushil.kakkar@bgiet.ac.in,*[3]*ravikantmail@rediffmail.com*

Abstract: MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs). In recent years, the device feature size of such circuits has been scaled down into the deep submicrometer range. In this paper, a 90 nm NMOS in 3-D structure was designed and simulated to study its electrical characteristics using Visual TCAD with GENIUS simulator. From the simulated result, optimum solution is found in which the value of threshold voltage is 0.2568 is achieved. The value is compared with ITRS guideline of 90nm device.

Keywords: Doping, Mesh, 90nm, Visual TCAD

I. Introduction

The gate length of high-performance MOSFETs has been aggressively scaled year by year because of a strong requirement for constant improvement of circuit performance. The history of the International Technology Roadmap for Semiconductors (ITRS) demonstrates how the gate length of high-performance MOSFETs was scaled in the past and was required to set the pace for scaling in the future [1]. This technology is now well-developed and similar processes of MOSFET fabrication are widely used in industry throughout the world [2]. The scaling of the Complementary Metal Oxide Semiconductor (CMOS) devices to smaller physical dimensions have became the driving force for the semiconductor industry to meet the market's demand for greater functionality and performance of the integrated circuit at a low cost [3]. Smaller MOSFETs are desirable by main reasons.

1. Smaller MOSFETs allow more current to pass, because of the low resistance.

2. Smaller MOSFETs have smaller gates, and thus lower gate capacitance.

These two factors provide lower switching times, and thus higher speeds. Gate oxide thickness, channel doping, channel length, are varying factors that controlling threshold voltage (V_T) and caused device performance problems [5] [6]. V_T is important parameter which determines whether transistor works or not [5].LDD and retrograde well are implemented to control short channel effect and hot carrier reliability [7]. Besides that, LDD is designed to smear out the strong electric field between the channel and heavily doped source or drain, in order to reduce hot carrier generation [5]. International Technology Roadmap for Semiconductor (ITRS) value in which V_T value should be 0.2685 ± 12.7% is being used as the target to achieve the objective of research.

II. Design and Materials

In MOSFET transistor the bottom rectangular block of material is the silicon substrate often referred to as the bulk. There are four electronically active regions that are marked: *gate* (G), *source* (S), and *drain* (D), and the *bulk* terminal (B) to which the gate, drain, and source voltages are typically referenced. The rectangular gate region lies on top of the bulk separated by a thin silicon oxide dielectric with thickness T_{OX}. Two other important dimensions are the transistor gate length and width. The drain and source regions are embedded in the substrate but have an opposite doping to the substrate. Device simulation is applied to calculate the electrical behaviour of semiconductor devices. Table 1 shows regions and materials used in simulation of device. Table 2 shows doping and profiles used in device.

Table 1. Regions and Material used in NMOS

Region	Material	Length/µm
Substrate	Silicon	0.29
Drain	Aluminium	0.10
Source	Aluminium	0.10
Gate	NpolySi	0.09
Oxide	Sio_2	0.35

Table 2. Doping Profile

Name	Profile	Type	DOPING
Substrate	Uniform	Acceptor	3E17
Channel	Gaussian	Acceptor	1E13
LDD_S/LDD_D	Gaussian	Donor	5E19
Source/Drain	Gaussian	Donor	2E20

III. Result and Discussion

The simulation results of 90 nm NMOS can be viewed in the Tony Plot is shown below. GENIUS code has flexible mesh data structure which supports various shapes of 2D and 3D elements. The only limit is the element should have circum-circle for 2D or circum-sphere for 3D to meet finite volume method used by GENIUS. The supported element shapes can be triangle and quadrangle for 2D, tetrahedron, prism and hexahedron for 3D. In this research triangle is used. Figure 1 show the mesh layout on which final structure of this MOSFET device is implemented. It is base of device. Figure 2 shows regions in device. Holes are majority carrier and electrons are minority carrier in p type semiconductor. Holes are minority carrier and electrons are majority carrier in n type semiconductor.

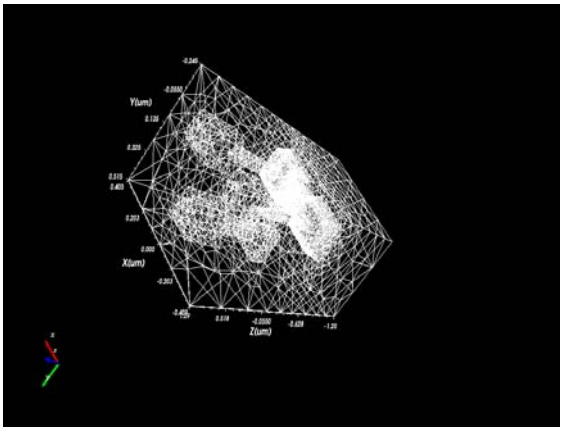

Figure 1: 90 nm device mesh in 3-D

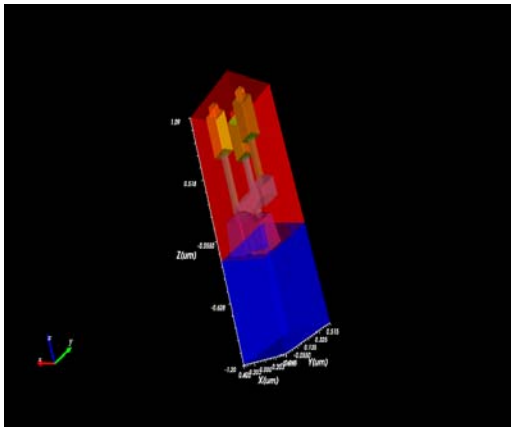

Figure 2:Region in device in 3-D

Figure 3 shows acceptor doping in device. Figure 5 shows donor doping in device. For simulation the transient response of device, GENIUS supports several types of voltage and current source. The original models of these sources come from SPICE, a famous circuit simulation program.

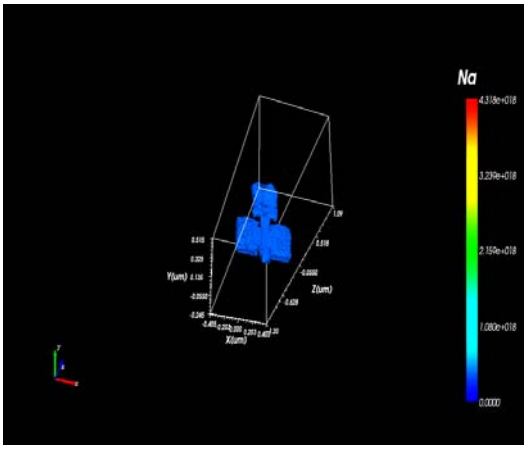

Figure 3: Acceptor doping in device

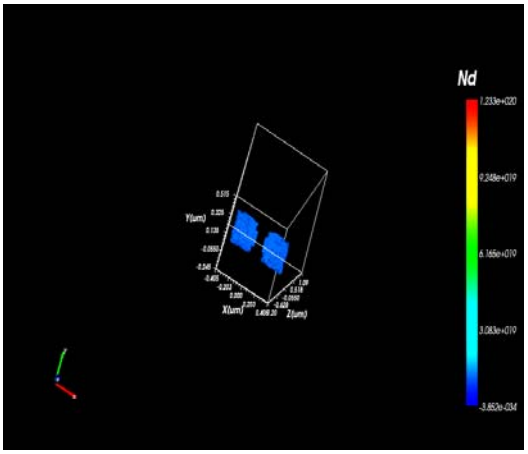

Figure 4: Donor doping in Device

Figure 5 shows the device structure without Sio_2 . Blue colour shows silicon substrate, yellow colour shows aluminium electrode. Figure 6 shows 90nm NMOS device.

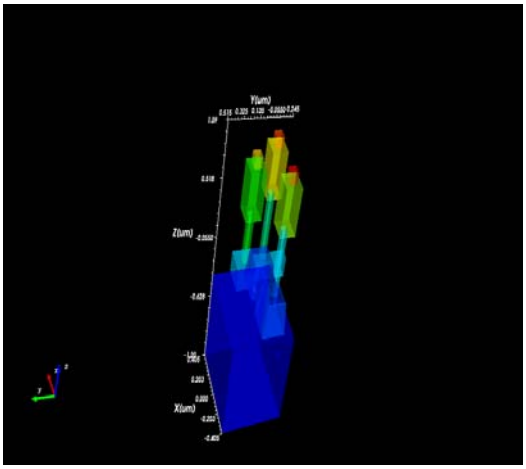

Figure 5: Device without Sio_2

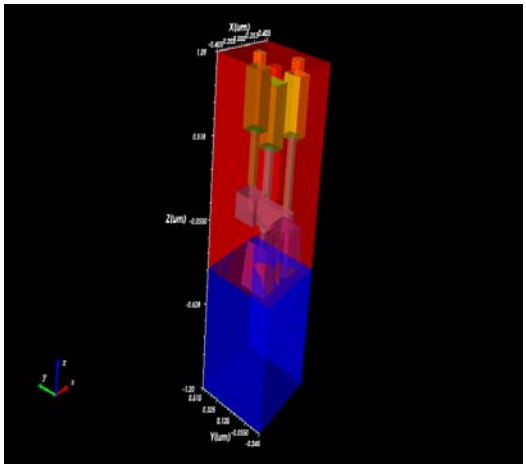

Figure 6: 90nm device in 3-D

Figure 7 shows that I_D versus V_{GS} curve for NMOS. By this curve, the value of threshold voltage (V_T) can be extracted. In this operation the threshold voltage happens when current reaches zero. V_D = 2V is applied for this device. When $V_G < V_T$, the current is zero but the current start increasing when $V_G > V_T$. With small value of V_{DS} applied it is possible to examine the effect of an increase gate voltage. Figure 8 show the families of I_D versus V_{DS} curve for NMOS. The curve is plotted using Visual TCAD with GENIUS simulator. From figure 5 it is observed that the V_T of NMOS device is 0.2568V

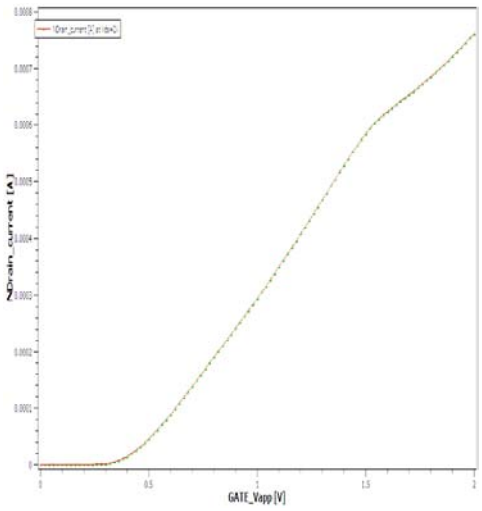

Figure 7: I_D versus V_{GS} at V_{DS}=2V

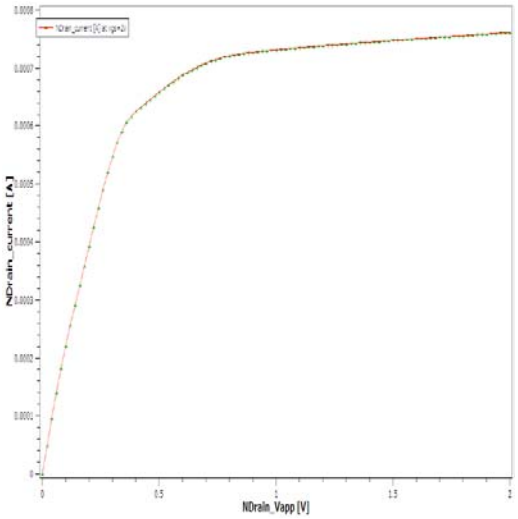

Figure 8: I_D versus V_{DS} at V_{GS}=2V

IV. CONCLUSION

The 90 nm is simulated by using Visual TCAD module. By using TCAD module, electrical response of the NMOS is to be simulated.V_{TH} is the main response studied in this project as it the main factor in determining whether a digital device works or not. From the simulation result, the optimum V_T value of 0.2568 V is obtained. The value is in line with ITRS guideline for 90 nm NMOS.

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