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TOPOLOGIES OF MULTILEVEL CONVERTERS: CONCEPT OF REDUNDANCY

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ABSTRACT: — Switching state redundancy provides flexibility in multilevel systems and may be used to achieve some control objectives such as capacitors voltage balancing, current control of dc-sources, switch power loss balancing and fault tolerance. This paper studies the per-phase redundancy in three basic multilevel topologies: diode-clamped converter, flying capacitor converter and cascaded bull-bridge converters. The number of per-phase redundant switching states, the rules for triggering each topology and the relationships among them are studied through this paper and simulation results are presented.

Keywords: *multilevel converter, redundancy , cascaded bridge inverter*

I. INTRODUCTION:

Redundancy is referred to as the capability of power converters to produce the same output voltages with different switching states. Two types of redundancy are possible: per-phase redundancy andjoint-phase redundancy . The joint-phase redundancy is present in converters with no neutral wire and does not depend on the converter topology. It is based on the fact that several different line-to-ground voltage combinations provide the same line-to-line voltage . Joint-phase redundancy has been studied in depth and it is well known in three-phase converters. In fact, space vector pulse-width modulation (SVPWM) techniques have become very popular in three-phase applications because their aptitude to manage it. Classical carrier-based sinusoidal pulse-width modulation (SPWM) techniques deal with joint-phase redundancy by means of a zero sequence offset added to the reference waveform of every phase. Different zero sequences lead to different modulation trategies with different performance levels. The equivalence between this zero sequence in SPWM and the SVPWM is studied in . Per-phase redundancy refers to certain power converter topologies that have redundant switching states within each phase , so that several transistor switching combinations lead to the same line-to-ground voltage. Per-phase redundancy can be used or combined with joint-phase redundancy in multilevel converters to achieve certain control objectives such as capacitors voltage balancing , current control of dc-sources , switch power loss balancing and increase in fault tolerance .

II. DIODE-CLAMPED CONVERTER

The diode-clamped converter [2, 3, 5] provides multiple voltage levels through the connection of the phases to a series bank of capacitors. According to the original invention [2], the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels

[3] where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral-point clamped (NPC) inverter was introduced [3]. However, with more than three levels the term diode-clamped topology is applied , Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to three-levels, and because of industrial developments over the past several years, it is now used extensively in industry applications .

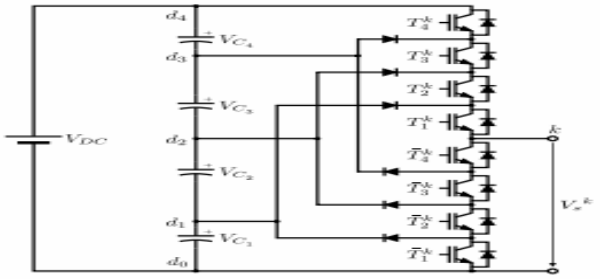


Figure 1.1 shows the topology of one phase of a five-level diode-clamped converter.

In summary, the dc-bus is split by means of series connected capacitors, and the phase node k can be connected to any node in the capacitor bank (d_0, d_1, d_2, $d_3$or d_4). In this representation, the labels $T_i k$ are used to identify the transistors as well as the semiconductor logic (1 = on and 0 = off). Since the transistors are always switched in pairs, to avoid short-circuiting of dc-link capacitors, the complementary pairs are labeled as T_i^k and T^{-}_i accordingly. In practical implementations, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition . However, for the discussion herein, the dead time will be ignored and it will be considered that the complementary trigger signals always sum to one:

$$T_i^k + \bar{T}_i^k = 1 \quad \text{.....(1)}$$

Hence, $T^{-}_i{}^k$ is the inverse of T_i^k and only one of the transistors in the pair is independent. The same consideration applies to the flying capacitor and the cascaded full-bridge topologies. If the power losses are neglected then the transistor blocking voltage VT_i^k in a multilevel topology is given by

$$V_{T_i^k} = (1 - T_i^k) V_{C_i} \quad \text{.....(2)}$$

Where V_{Ci} is the voltage of the capacitors in the bank. For every converter level, it must be taken into account that if $T_{i=0}^k$ then $T^k_{i=1}= 0$. The output voltage of one phase V_s can be calculated from transistor voltages by means of

$$V_s^k = V_{DC} - \sum_{i=1}^{N^k-1} V_{T_i^k} \quad \text{.....(3)}$$

Where N^k is the number of levels of the phase k of the converter, and V_{DC} is the full dc link voltage. If (2) is substituted in the above expression then the output voltage can be obtained from the trigger signals as

$$V_s^k = \sum_{i}^{N^k-1} T_i^k V_{C_i}, \quad \text{where if } T_i^k = 0 \text{ then } T_{i+1}^k = 0. \quad \text{.....(4)}$$

Usually, all capacitors in the bank are equally charged

$$V_{C_i} = \frac{V_{DC}}{N^k - 1} = V_{dc}, \quad \text{for all } i. \quad \text{.....(5)}$$

In this case (2) & (4) equations can be rewritten as

$$V_{T_i^k} = (1 - T_i^k)V_{dc}$$

$$V_s^k = V_{dc} \sum_{i=1}^{N^k-1} T_i^k \quad \text{.....(6)}$$

Since the result of the summation term is always an integer number, the output voltage is an integer multiple of fixed voltage V_{dc}.

$$V_s^k = v_s^k V_{dc}, \qquad \text{where } v_s^k \in \mathbb{N}. \quad \text{.....(7)}$$

T_1^k	T_2^k	T_3^k	T_4^k	V_s^k	V_s^k (if $V_{C_i} = V_{dc}$)	v_s^k
0	0	0	0	0	0	0
1	0	0	0	V_{C_1}	V_{dc}	1
1	1	0	0	$V_{C_1} + V_{C_2}$	$2V_{dc}$	2
1	1	1	0	$V_{C_1} + V_{C_2} + V_{C_3}$	$3V_{dc}$	3
1	1	1	1	$V_{C_1} + V_{C_2} + V_{C_3} + V_{C_4}$	$4V_{dc}$	4

Table: five level Diode clamped converter relationships

Therefore, V_{dc} and v_{sk} are the voltage step and the output level of the converter, respectively. The output level can be calculated from the switching state by means of

$$v_s^k = \sum_{i=1}^{N^k-1} T_i^k, \qquad \text{where if } T_i^k = 0 \text{ then } T_{i+1}^k = 0. \quad \text{.....(8)}$$

Table shows the trigger signals, output voltages and output levels corresponding to the five-level converter in Figure 3.1.

III. FLYING-CAPACITOR CONVERTER

Another fundamental multilevel topology is the flying capacitor converter, which involves series connection of capacitor clamped switching cells [6]. In this topology the voltage clamping is achieved by means of capacitors that float with respect to the ground..Figure 1.2 shows the structure for one phase of a five-level flying capacitor converter.Neglecting the device voltage drop as well as conductions losses, the blocking voltage of each switch V_{Ti}^k depends on the voltage of the floating capacitor V_{Ci}^k as

$$V_{T_i^k} = (1 - T_i^k)(V_{C_i^k} - V_{C_{i-1}^k}) \quad \text{.....(9)}$$

The phase output voltage V_S^k can be calculated from the transistor

$$V_s^k = V_{C_{N^k-1}^k} - \sum_{i=1}^{N^k-1} V_{T_i^k} \quad \text{.....(10)}$$

If (9) is substituted in the above expression then the output voltage can be obtained from the trigger signals as

$$V_s^k = \sum_{i=1}^{N^k-1} T_i^k (V_{C_i^k} - V_{C_{i-1}^k}), \qquad \text{where } V_{C_0^k} = 0 \text{ and } V_{C_{N^k-1}^k} = V_{DC}. \quad \text{.....(11)}$$

Usually, the flying capacitors voltage is an integer multiple of a fixed voltage V_{dc}:

$$V_{C_i^k} = iV_{dc}, \qquad i \in \mathbb{N}. \quad \text{.....(12)}$$

In this case (9) & (11) equations can be simplified as

$$V_{T_i^k} = (1 - T_i^k)V_{dc}$$

$$V_s^k = V_{dc} \sum_{i=1}^{N^k-1} T_i^k \quad \text{.....(13)}$$

Since the result of summation term is always an integer number, the output voltage is an integer multiple of the fixed voltage V_{dc}:

$$V_s^k = v_s^k V_{dc}, \qquad \text{where } v_s^k \in \mathbb{N} \quad \text{.....(14)}$$

Therefore, V_{dc} and $v_s$kare the voltage step and the output level of the converter, respectively. Hence, the relationship between the output level v_sk and the switching state is

$$v_s^k = \sum_{i=1}^{N^k-1} T_i^k \quad \text{.....(15)}$$

Therefore, there are different combinations of T_i^k that provide the same output level. This redundancy gives great flexibility in the selection of the transistors that must be switched to obtain a particular output level.

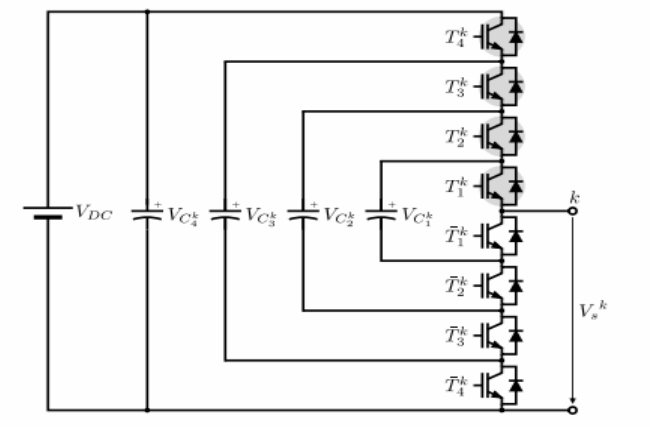


Figure 1.2: Five-level flying capacitor converter.

T_1^k	T_2^k	T_3^k	T_4^k	V_s^k	V_s^k (if $V_{C_i^k} = iV_{dc}$)	v_s^k
0	0	0	0	0	0	0
1	0	0	0	$V_{C_1^k}$	V_{dc}	1
0	1	0	0	$V_{C_2^k} - V_{C_1^k}$	V_{dc}	1
0	0	1	0	$V_{C_3^k} - V_{C_2^k}$	V_{dc}	1
0	0	0	1	$V_{C_4^k} - V_{C_3^k}$	V_{dc}	1
1	1	0	0	$V_{C_2^k}$	$2V_{dc}$	2
1	0	1	0	$V_{C_3^k} - V_{C_2^k} + V_{C_1^k}$	$2V_{dc}$	2
1	0	0	1	$V_{C_4^k} - V_{C_3^k} + V_{C_1^k}$	$2V_{dc}$	2
0	1	1	0	$V_{C_3^k} - V_{C_1^k}$	$2V_{dc}$	2
0	1	0	1	$V_{C_4^k} - V_{C_3^k} + V_{C_2^k} - V_{C_1^k}$	$2V_{dc}$	2
0	0	1	1	$V_{C_4^k} - V_{C_2^k}$	$2V_{dc}$	2
1	1	1	0	$V_{C_3^k}$	$3V_{dc}$	3
1	1	0	1	$V_{C_4^k} - V_{C_3^k} + V_{C_2^k}$	$3V_{dc}$	3
1	0	1	1	$V_{C_4^k} - V_{C_2^k} + V_{C_1^k}$	$3V_{dc}$	3
0	1	1	1	$V_{C_4^k} - V_{C_1^k}$	$3V_{dc}$	3
1	1	1	1	$V_{C_4^k}$	$4V_{dc}$	4

Table: Five-level flying capacitor bridge converter relationships.

IV. CASCADED FULL-BRIDGE CONVERTER

The cascaded full-bridge converter was the first invented multilevel topology [1].

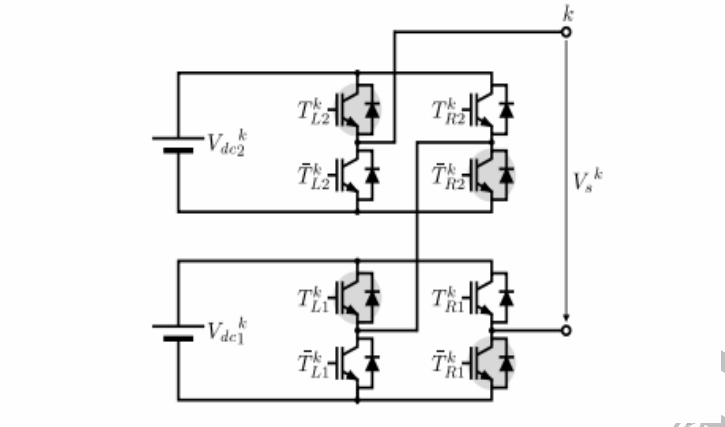


Figure 1.3: Five-level cascaded full-bridge converter

Early uses of the topology were devoted to single-phase applications . Later, this approach was extended to include three-phase systems. The cascaded full-bridge converter consists of series full-bridge cells. Since each cell can provide three voltage levels (zero, positive dc voltage, and negative dc voltage), the cells are themselves multilevel converters. A phase of a two-cell series full-bridge inverter is shown in Figure 1.3.

If device voltage drops and conduction losses are neglected then the phase output voltage of one phase is given by the below equation.

$$V_s^k = \sum_{i=1}^{B^k} (T_{Li}^k - T_{Ri}^k) V_{dci}^k \quad \text{.....(16)}$$

Where B^k is the number of cascaded cells, T_{Li}^k and T_{Ri}^k are the trigger signals of the transistor placed left and right, respectively, in cell i, and V_{dci}^k is the dc source corresponding to the same cell. The semiconductor blocking voltages can be calculated from the switching states by mean of

$$V_{T_{Li}^k} = (1 - T_{Li}^k) V_{dci}^k$$
$$V_{T_{Ri}^k} = (1 - T_{Ri}^k) V_{dci}^k \quad \text{.....(17)}$$

Usually, all independent voltage sources are equal:

$$V_{dci}^k = V_{dc} \quad \text{.....(18)}$$

In this case (16) equation can be rewritten as

$$V_s^k = V_{dc} \sum_{i=1}^{B^k} (T_{Li}^k - T_{Ri}^k) \quad \text{.....(19)}$$

Since the result of the summation term is always an integer number, the output voltage is an integer multiple of fixed voltage V_{dc}

$$V_s^k = v_s^k V_{dc}, \qquad \text{where } v_s^k \in \mathbb{Z} \quad \text{.....(20)}$$

Therefore, V_{dc} and V_s^k are the voltage step and the output level of the converter, respectively. Hence, the relationship between the output level V_s^k and the switching state is

$$v_s^k = \sum_{i=1}^{B^k} (T_{Li}^k - T_{Ri}^k) \quad \text{.....(21)}$$

Table: Five-level cascaded full-bridge converter relationships.

T_{L1}^k	T_{L2}^k	T_{R1}^k	T_{R2}^k	V_s^k	V_s^k (if $V_{dc_i}^k = V_{dc}$)	v_s^k
0	0	1	1	$-V_{dc_2}^k - V_{dc_1}^k$	$-2V_{dc}$	-2
1	0	1	1	$-V_{dc_2}^k$	$-V_{dc}$	-1
0	1	1	1	$-V_{dc_1}^k$	$-V_{dc}$	-1
0	0	0	1	$-V_{dc_2}^k$	$-V_{dc}$	-1
0	0	1	0	$-V_{dc_1}^k$	$-V_{dc}$	-1
1	1	1	1	0	0	0
1	0	0	1	$V_{dc_1}^k - V_{dc_2}^k$	0	0
1	0	1	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	$V_{dc_2}^k - V_{dc_1}^k$	0	0
0	0	0	0	0	0	0
1	1	0	1	$V_{dc_1}^k$	V_{dc}	1
1	1	1	0	$V_{dc_2}^k$	V_{dc}	1
1	0	0	0	$V_{dc_1}^k$	V_{dc}	1
0	1	0	0	$V_{dc_2}^k$	V_{dc}	1
1	1	0	0	$V_{dc_2}^k + V_{dc_1}^k$	$2V_{dc}$	2

Since this topology can generate levels going from $-B^k$ to B^k then the number of different output levels is

$$N^k = 2B^k + 1. \quad \text{.....(22)}$$

Thus, if all voltage sources are equal then this kind of converters always provides an odd number of levels. Even so, it is possible to achieve an even number of levels if a half-bridge is added to the chain of full-bridge cells.

Table shows the switching signals, output voltages and possible levels for the converter in Figure 1.3.

V. SWITCHING STATE REDUNDANCY

The proper switching states to obtain a particular converter output level can be obtained from equations. Such equation, like in the flying capacitor topology, has no unique solution. It only establishes the following switching law to select the transistors that must be turned-on:

> "The subtraction of the number of independent switches chosen from the left side branches of the converter and those that are chosen from the right side has to be equal to the numeric value of the output level."

There are no restrictions for carrying this selection since one equtation does not establish priorities among switches.

If (1) & (21) substituted, the following equivalent expression is obtained

$$v_s^k + B^k = \sum_{i=1}^{B^k} (T_{Li}^k + \bar{T}_{Ri}^k). \quad \text{.....(23)}$$

This new expression provides an alternative law for choosing the switches that must be turned-on:

"Among the switches of the right hand side branches and the complementary ones of the left side branch, a number $B^k + v_s k$ of independent switches must be selected to

$v_s k$."

For example, to get the level $v_s k_{=1}$ in the converter in Figure 3.3, three switches ($v_s k_{+} B^k = 1 + 2$) must be turned-on among the highlighted ones. Therefore, $B^k + v_s k$ switches must be chosen in a set of $2B^k$ elements to obtain the level $v_s k$. Hence the number of redundant states corresponding to the level $v_s k$ is given by

$$R_d(v_s{}^k) = \binom{2B^k}{B^k + v_s{}^k} = \frac{(2B^k)!}{(B^k - v_s{}^k)!\,(B^k + v_s{}^k)!} \quad \text{.....(24)}$$

Table: Number of per-phase redundant switching states in multilevel cascaded full-bridge converters.

	$R_d(-4)$	$R_d(-3)$	$R_d(-2)$	$R_d(-1)$	$R_d(0)$	$R_d(1)$	$R_d(2)$	$R_d(3)$	
$B^k = 1$	–	–	–	1	2	1	–	–	–
$B^k = 2$	–	–	1	4	6	4	1	–	–
$B^k = 3$	–	1	6	15	20	15	6	1	–
$B^k = 4$	1	8	28	56	70	56	28	8	1

Table shows the number of redundant states for each output level in multilevel cascaded full-bridge converters.

The number $S_w i \rightarrow j$ of semiconductors that must be switched to change the output from level $v_s i$ to level $v_s j$ can be obtained by means of

$$S_{w_i^k \rightarrow j} \geq 2|v_{s_i}^k - v_{s_j}^k| \quad \text{.....(25)}$$

A. CHARACTERISTICS

Important advantages of this topology are the following:

• The main important feature is its great modularity. Since this topology consists of series-connected power conversion cells, the voltage and power level may be easily scaled adding new cells.

• This topology, like flying capacitor, also presents per-phase redundancy that can be used for dc sources current control and switch loss balancing.

• At expense of reducing per-phase redundancy, the number of output levels can be increased, without adding new components, by using dc sources of di□erent voltages. This approach can be implemented with hybrid device technology where the slower and higher-voltage devices are used to change the output voltage level, while the faster and lower-voltage devices provide the full PWM capability .

Nevertheless, the fact that the dc-link voltages must be isolated is the major drawback for application of this topology. Several independent dc power supplies are required, which can be provided either by a transformer with multiple isolated secondary windings or by several transformers . Batteries , fuel cells , capacitors , or photovoltaic panels ,can also be used as independent dc sources.

B. REDUNDANT SWITCHING STATE SELECTION

If above expressions are compared then it can be concluded that in the three previous multilevel topologies the output voltage is an integer multiple of a fixed voltage V_{dc}:

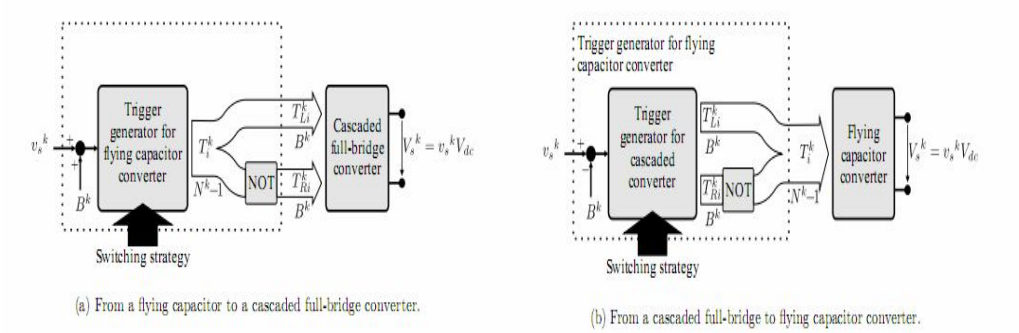
$$V_s^k = v_s^k V_{dc}, \qquad v_s^k \in \mathbb{Z} \quad \text{.....(26)}$$

This is a very important property because it makes it possible to use the same SVPWM with the three topologies. In addition, because of this property, the switching vectors $v_s 1 = [V_S^1 \ldots V_S^P]^T$ $V_S^2 = [V_S^{1+n}, v_s 2_{+n}, \ldots, V_S^{P+n}]^T$ provide the same line-to-line voltages; hence, it is also the basis of the joint-phase redundancy in multilevel converters. The new multilevel multiphase SVPWM presented. Joint-phase redundancy is further investigated, where a new SVPWM algorithm that allows to choose redundant switching states is developed.

Once the converter output level of each phase $v_s k$ has been obtained from the multilevel modulator, the transistor trigger signals must be determined. As it was shown in sections above, the relationship between output levels and the trigger signal is di□erent for each topology. Therefore, this task must be specifically developed for each topology. In the diode-clamped topology there is no per-phase switching state redundancy. The one-to-one relationship between output levels and trigger signals, can be implemented by means of a lookup table. Consequently, switching strategies in diode-clamped converters can be

only implemented by using joint-phase redundancy. In the flying capacitor and cascaded full-bridge topologies, there is no one-to-one correspondence between out-put levels and trigger signals; therefore, a redundant switching state selection technique is required. Although switching laws of the three topologies are di□erent, they have some similarities that allow establishing some relationship among them.

Flying capacitor converters and cascaded full-bridge converters that have the same number of levels also have the same number of controlled switches, and the number of redundant switching states follows the same profile. In addition, the switching laws derived from (15) & (23),have also the same form in both topologies. Consequently, it is possible to adapt the trigger generator of a flying capacitor converter to be used with a cascaded full-bridge converter with the same number of levels, and vice versa.



(a) From a flying capacitor to a cascaded full-bridge converter.

(b) From a cascaded full-bridge to flying capacitor converter.

Figure : Trigger generator adaptation between flying capacitor and cascaded full-bridge Topologies

If expressions are compared then following corrections are needed to trigger a cascaded full-bridge converter by means of a trigger generator of a flying capacitor converter:

1.The desired output level in the cascaded full-bridge converter $v_s k$ must be shifted by its number of cells B^k.
2.Next, the trigger signals provided by the generator $T_i k$ must be divided in two groups:
(a)The first group $T_{Li}k$ will drive the left branch switches of the cascaded full-bridge converter.
(b)The inverse signals of the second group $T_{Ri}k$ will drive the right branch switches of the converter.

The switching laws of both topologies do not make distinctions among switches, therefore it does not matter how the signals are grouped and assigned to the transistors in each cell. Obviously, the switching strategy for capacitor balancing in the flying capacitor topology is useless in a cascaded full-bridge converter; therefore, the switching strategy must be updated taking into account the particular transistor trigger signal assignment.

1. The desired output level in the flying capacitor converter $v_s k$ must be shifted by the negative number of cells $-B^k$.
2. Next, the trigger signals corresponding to the transistors in the right branch of the full-bridge converter $T_{Ri}k$ must be inverted.
3. Finally, the trigger signals for the flying capacitor converter $T_i k$ are obtained by grouping all the resulting trigger signals.

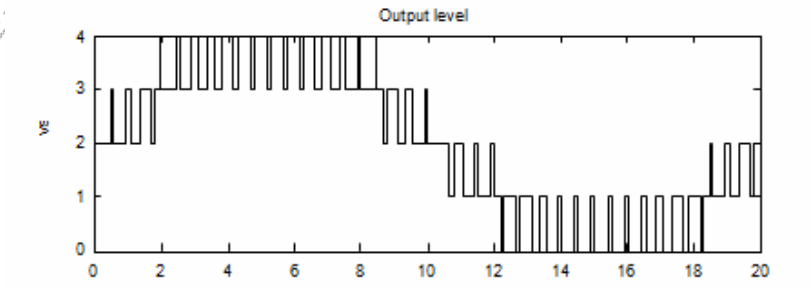
It does not matter how the signals are grouped and assigned to the power switches. Table verifies the proposed technique with two five-level converters. It compares the trigger signals corresponding to the flying capacitor converter with trigger signals and of the cascaded full-bridge converter. Both topologies have the same number of transistors, and

the levels that di□er by two units (B^k= 2) have equivalent switching states. A similar table and the same conclusion would be obtained if other groups of signals were compared.

Expressions related to a flying capacitor converter with an additional constraint. herefore, a trigger generator designed for diode-clamped converters, which implements can be used with a flying capacitor converter with the same number of levels. And, consequently, it can also be adapted to be used with a cascaded full-bridge converter. Nevertheless, since the diode-clamped converter does not have per-phase redundancy, if its trigger generator is used with a flying capacitor or with a cascaded full-bridge converter then it is not possible to take advantage of per-phase redundancy present in those topologies. Hence, capacitor balancing, current control of dc sources and switch loss balancing must be carried out by using alternative methods. As The trigger signals for a flying capacitor converter or a cascaded full-bridge onverter cannot be adapted to a diode-clamped converter because the extra constraint in the switching law of the latter converter is not observed by the trigger generators designed for the former converter.

Figure 1.4 shows the simulation results of using a trigger generator for a diode-clamped converter with flying capacitor and cascaded full bridge converters. Capacitors have been substituted with dc sources to avoid voltage imbalances.100 V dc sources have beenused. The first plot is the converter output level v_sk provided by the multilevel modulator.Second plot is the PWM output voltage (thick line) corresponding to a five-level diode-clamped converter. It has been obtained with the trigger signals (thin lines), T_4k, T_3k, T_2k and T_1k, that have been calculated by means of (2.10). Third plot is the output voltage V_sk (thick line) of a five-level flying capacitor converter when the trigger generator for the diode-clamped converter is used with it. As Figure 2.5a shows, the same trigger signals (thin lines) are directly used. Last plot is the output voltage V_sk (thick line) of a five-level cascaded full-bridge converter when the trigger generator for the diode-clamped converter has been adapted to be used with it. The reference output level has been shifted to fitthe output voltage in the range [−200 V, 200 V]. The four trigger signals (thin lines), T_Lk_2, T_Lk_1, $T_Rk_2$and T_Rk_1, have been adapted using the scheme in Figure 2.5b. The output voltages of all multilevel converters are equal, which validates the proposed adaptation techniques.

VI. RESULTS:



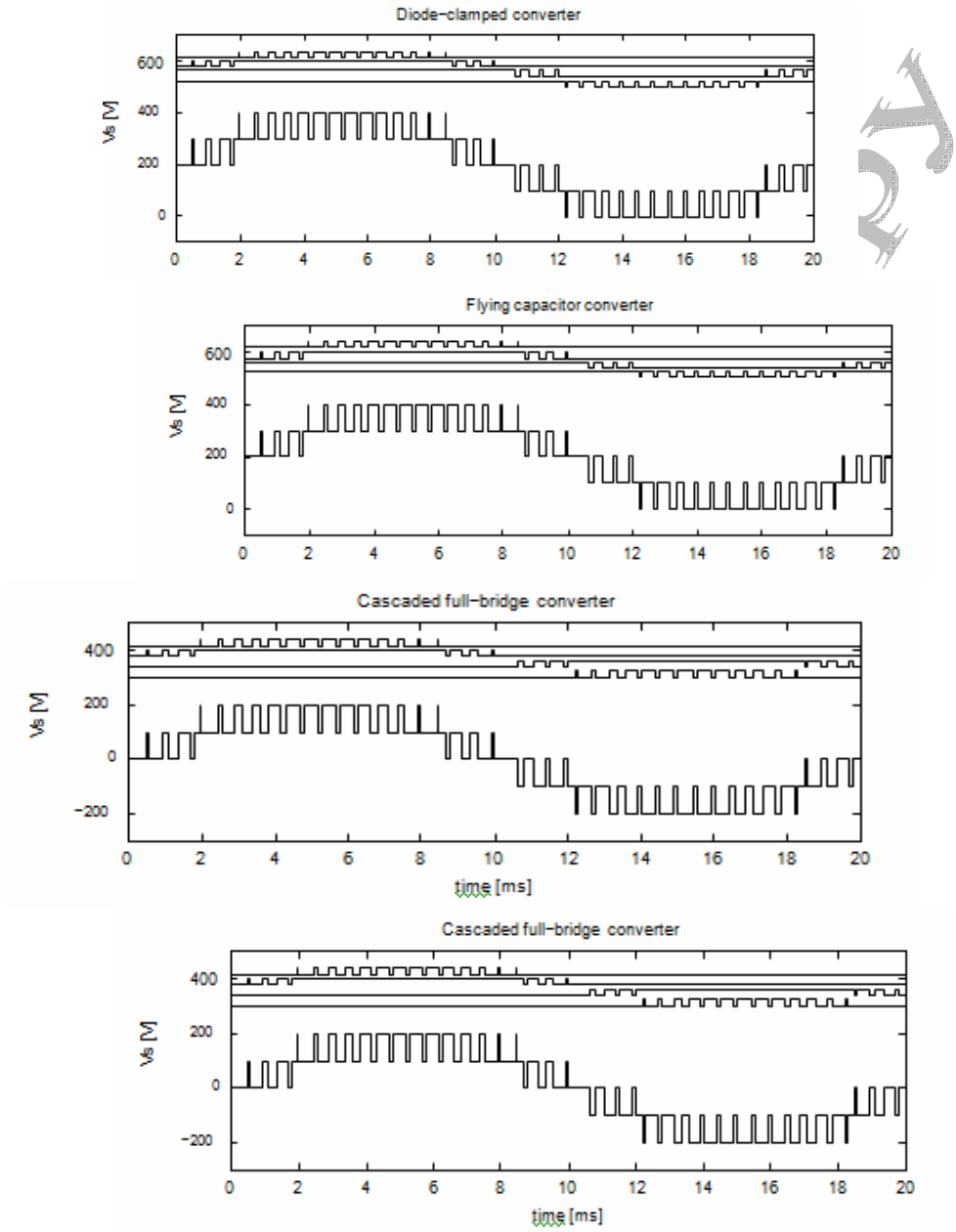


Figure 1.4: Simulation results of using a trigger generator for a diode-clamped converter with a flying capacitor and a cascaded full bridge converter.

VII. CONCLUSION

In this paper the per-phase switching state redundancy in the three main multilevel topologies has been studied. Contributions of the paper include new expressions to calculate the number of redundant switching states of each output level in the diode- clamped, flying capacitor and cascade full-bridge topologies, and the switching laws for triggering them. Those laws have been used to study the relationships among the trigger generators of the multilevel topologies concluding that:

- The trigger generator of a diode-clamped converter can be used with a flying capacitor or a cascaded full-bridge converter sacrificing their per-phase redundancy. The inverse task is not possible.

- The trigger generator for a flying capacitor converter can be adapted to be used

with a cascaded full-bridge converter and vice versa.

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